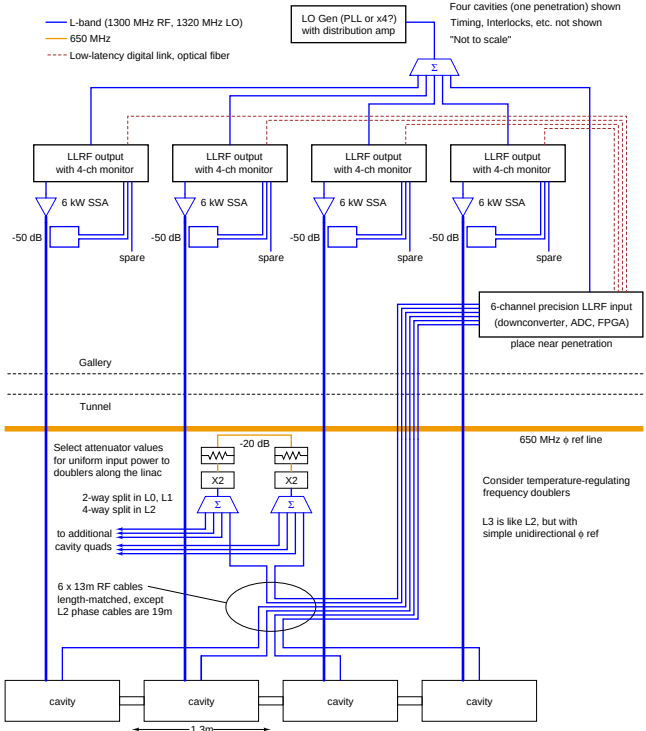
LCLS-II LLRF Architecture

Larry Doolittle, LBNL, 2014-12-03

LCLS-2 LLRF Hardware Architecture Concept

Larry Doolittle, 2014-04-14, revised 2014-10-30



All long cables and analog components are phase-drift compensated

• Digital variant of field-tested phase-averaging reference line used for ∼150 m runs covering L0, L1, and L2

• Matched 13 m cables move probe and reference signals up to gallery in L0 and L1

• Precision receiver channels will approximately track each other in phase (this can be checked on the bench), and the receiver temperature stabilization upgraded if needed (starts in an air-conditioned rack)

• Explicitly depends on beam-based feedback (slow is OK) to remove residual drift

• No drift compensation in L3 (but that linac operates on-crest)

Brings up "raw" probe cables for commissioning and troubleshooting

Simpler than more exotic phase calibration schemes

By centralizing precision receiver:

• Keep microphonically varying forward and reverse RF signals away from the critical probe RF

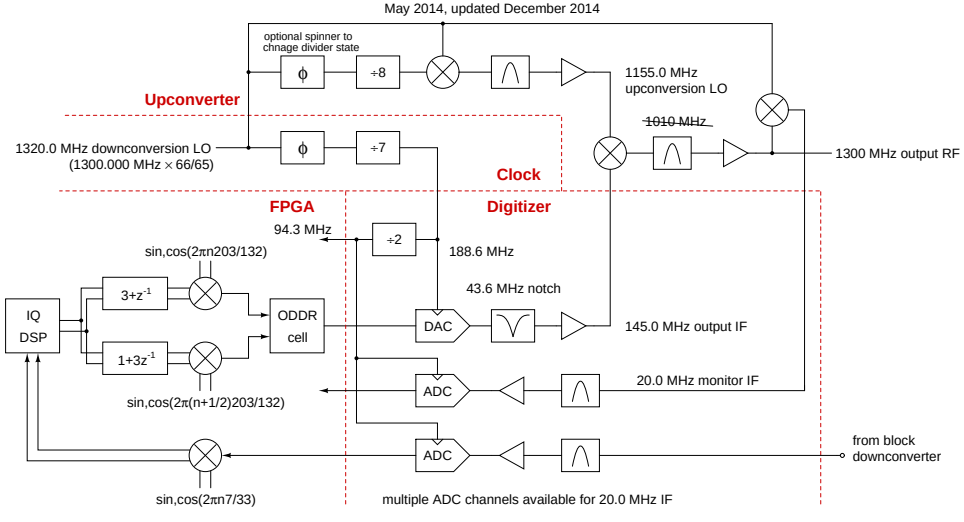
• Digitally duplicate the reference digitizer result across four stations

• Isolate the most sensitive measurements from most sources of EMI

• Add "only" about 140 ns to field control loop latency

• LO must be shared between receiver and control station (cable drift is OK)

LCLS-2 1300 MHz Clocking and Frequency Conversion Concept



$$f_{\mathrm{RF}} = 1300 \text{ MHz}$$
$$f_{\mathrm{Clk}} = 94.3 \text{ MHz} = f_{\mathrm{LO1}}/14$$
$$f_{\mathrm{IF1}} = \ \ 20 \text{ MHz} = f_{\mathrm{Clk}} \cdot \tfrac{7}{33}$$
$$f_{\mathrm{LO1}} = 1320 \text{ MHz}$$
$$f_{\mathrm{IF2}} = \ 145 \text{ MHz} = f_{\mathrm{Clk}} \cdot \tfrac{203}{132}$$
$$f_{\mathrm{LO2}} = 1155 \text{ MHz} = f_{\mathrm{LO1}} \cdot (1 - \tfrac{1}{8})$$

Unusual Split-LO design bypasses usual compromises in choosing IF

- Low 20 MHz IF for receiver reduces crosstalk and sensitivity to ADC clock jitter
- High 145 MHz IF for transmitter improves options for output sideband-select filter
- Circumvents usual problems with isolation between drive and input IF
- Receiver IF near middle of first Nyquist zone of 94.3 MS/s ADC
- Full TM_{010} passband (1274-1300 MHz) fits in first Nyquist zone of ADC
- Transmitter IF near middle of second Nyquist zone of 188.6 MS/s DAC

Every 1820 RF cycles, we have 132 Clk cycles, 28 IF cycles, 203 IF2 cycles. Physically, that repeat period is 1.4 μs.

Coherent with larger LCLS timing system

- Gun will fill (or not) 1 RF bucket out of 1400
- 71.43 kHz synchronization point every 18200 cycles of 1300 MHz (LCLS-2), and every 6664 cycles of 476 MHz (LCLS-1)

Field control

- In equilibrium can be analyzed as PI control, with latency

50	ns	input analog BPF
130	ns	ADC pipe (12 cycles at 94.3 MHz)
64	ns	Precision Rx DSP (12 cycles at 188.6 MHz)
140	ns	GTP and fiber latency
106	ns	Controller DSP (20 cycles at 188.6 MHz)
530	ns	bandpass filter in DSP (300 kHz)
70	ns	notch filter in DSP ($\sim$800 kHz for $8\pi/9$ mode)
20	ns	DAC
20	ns	sideband selection filter
70	ns	L-band analog gain stages
100	ns	high-power RF cavity filter (1.6 MHz bandwidth)
50	ns	cables and waveguides
80	ns	contingency
1430	ns	total, can sustain 70 kHz closed loop bandwidth

Resonance control

- Computations done in LLRF FPGA based on RF measurements
- Results sent to Piezo and Stepper hardware for actuation